

REMARKS

This responds to the Office Action mailed on March 8, 2005.

Claims 1, 8, and 27 are amended, claims 4, 5 and 14-26 are canceled, and claims 31-37 are added; as a result, claims 1-3 and 6-13 and 27-37 are now pending in this application.

Information Disclosure Statement

Applicant submitted an Information Disclosure Statement and a 1449 Form on March 19, 2004. Applicant respectfully requests that an initialed copy of the 1449 Form be returned to Applicant's Representatives to indicate that the cited references have been considered by the Examiner.

§102 Rejection of the Claims

Claims 1-5 and 7-13 were rejected under 35 USC § 102(b) as being anticipated by Coico et al. (U.S. 6,354,844). Applicant has amended claims 1 and 8, from which claims 2-5, 7, and 9-13 depend to more clearly distinguish Applicant's claims from that which is disclosed by Coico et al. Applicant respectfully traverses the rejection.

Coico et al. disclose a Land Grid Array (LGA) electronic package/circuit board assembly (Figs. 1 and 2; col. 3, lines 10-12). The LGA package includes a pair of alignment pins 23 and 24 fabricated on selected ones of pads 17 on a substrate 5. (Fig. 1; col. 3, lines 36-39). The alignment pins 23 are to accurately and simply align the two-dimensional array of contact pads 17 on the substrate 5 with the two-dimensional array of conductive pins 19 on a flexible interposer 21. (Fig. 1, lines 31-36).

Applicant's claims 1-5 and 7 include at least the following features, which are not disclosed by Coico et al.:

"... at least one conductive, low insertion force, insertable feature extending perpendicularly from the first surface in a vertical direction, wherein the at least one conductive, low insertion force, insertable feature contacts conductive structures within the electronic circuit

package, and wherein the at least one conductive, low insertion force, insertable feature is configured to receive a horizontal force, provided by a horizontal force mechanism, to engage the at least one conductive, low insertion force, insertable feature with a receptacle.” (claim 1, as amended)

Regarding claims 1-5 and 7, nowhere do Coico et al. disclose a conductive, low insertion force, insertable feature configured to receive a horizontal force to engage the insertable feature with a receptacle, as is claimed in Applicant’s claims 1-5 and 7. The Office Action states that Coico et al., in col. 4, lines 55-63 disclose “the insertable feature 23 (fig. 1) could be a low insertion force feature.” However, Applicant respectfully disagrees. A low insertion force feature is a specific type of feature, which may be inserted into a receptacle through minimal vertical actuation force, and which remains engaged with the receptacle through a horizontal force applied by a horizontal force mechanism (see Specification, p. 2, lines 15-16, and p. 18, lines 1-6). Coico et al. states, in col. 4, lines 55-63:

“When assembled, alignment pins 23 and 24 are engaged in alignment holes 35 and 37 and clamping screws 39 and 41 are appropriately tightened into threaded holes 43 and 45 in backing plate 47 through holes 49 and 51 in circuit board 25. When tightened in place, pressure plate 15 applies sufficient force to substrate 5 to cause pins 19 in interposer 21 to variously minimally compress . . .”

In other words, the assembly of Coico et al. includes members (e.g., backing plate 47, clamping screws 39, 41, etc.) which apply a sustained vertical force to compress the assembly together. Nowhere does Coico et al. disclose low insertion force features.

Applicant’s claims 8-13 include at least the following features, which are not disclosed by Coico et al.:

“. . . a rigid body having a first surface;

at least one non-insertable contact having contact portions exposed at the first surface of the rigid body; and

at least one insertable contact having openings on the first surface and internal conductive structures within the rigid body. . ." (claim 8, as amended)

Regarding claims 8-13, nowhere do Coico et al. disclose a rigid body having a first surface, at least one non-insertable contact having contact portions exposed at the first surface, or at least one insertable contact having openings on the first surface and internal conductive structures within the rigid body. In contrast, Coico et al. disclose a two-dimensional array of conductive pins 19 on a flexible interposer 21. (Fig. 1, lines 31-36).

Coico et al. do not disclose all of the features of Applicant's claims. Applicant believes that the rejection of claims 1-5 and 7-13 under 35 USC § 102(b) has been overcome. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection , and allow claims 1-5 and 7-13.

§103 Rejection of the Claims

Response to Rejection of Claim 6:

Claim 6 was rejected under 35 USC § 103(a) as being unpatentable over Coico et al. in view of Liang (U.S. 5,532,612). Applicant has amended claim 1, from which claim 6 depends, and respectfully traverses the rejection.

Liang discloses a microprocessor that may include from 500 to 1000 terminals. (col. 1, lines 22-40).

Claim 6 is dependent from claim 1, which Applicant believes to be allowable over Coico et al. Claim 6 includes the following features:

" . . . at least one conductive, low insertion force, insertable feature extending perpendicularly from the first surface in a vertical direction, wherein the at least one conductive, low insertion force, insertable feature contacts conductive structures within the electronic circuit package, and wherein the at least one conductive, low insertion force, insertable feature is configured to receive a horizontal force, provided by a horizontal force mechanism, to engage the at least one conductive, low insertion force, insertable feature with a receptacle . . . (claim 1)

. . . wherein a total feature count is greater than 400 features, and the total feature count is a sum of a first number of non-insertable features and a second number of insertable features.”

(claim 6)

Neither Coico et al., Liang, nor their combination disclose, suggest or motivate the limitations of claim 6. More particularly, neither Coico et al, Liang, nor their combination disclose, suggest or motivate a conductive, low insertion force, insertable feature configured to receive a horizontal force to engage the insertable feature with a receptacle, which has a total feature count greater than 400 features, as is claimed in Applicant’s claim 6.

Further, there is no motivation given to combine Coico et al. and Liang. The Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Applicant respectfully submits that the Office Action has not provided objective evidence for a suggestion or motivation to combine the references.

For at least the above reasons, Applicant believes that the rejection of claim 6 under 35 USC § 103(a) has been overcome. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection , and allow claim 6.

Response to Rejection of Claims 27-30:

Claims 27-30 were also rejected under 35 USC § 103(a) as being unpatentable over Coico et al. in view of Kabadi et al. (U.S. 2003/0168738). Applicant has amended claim 27, from which claims 28-30 depend, and respectfully traverses the rejection.

The present application was filed on 6/27/2003. Kabadi et al. was filed on 3/8/2002 and published on 9/11/2003. Accordingly, Kabadi et al. may previously have been considered prior art under former 35 U.S. C. 103 via 35 U.S.C. 102(e). However, Kabadi et al. was, at the time the invention was made, owned by the same entity (Intel Corporation) or subject to an obligation of assignment to the same entity. Accordingly, Applicants believe that Kabadi et al. should be disqualified as prior art against the claimed invention.

For at least the above reason, Applicant believes that the rejection of claims 27-30 under 35 USC § 103(a) has been overcome. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection , and allow claims 27-30.

Support for Claim Amendments

Amendments to claim 1 are supported in the Specification at page 4, lines 24 through page 5, line 3, and at page 17, line 26 through page 18, line 6.

Amendments to claims 8 and 27 are supported in the Specification at page 16, lines 8-27, and at page 6, lines 16-24.

New Claims 31-37

New claims 31-37 include features disclosed in the Specification and/or claimed in the original claims 1-13, and add no new matter.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/608,050

Filing Date: June 27, 2003

Title: HYBRID PACKAGE WITH NON-INSERTABLE AND INSERTABLE CONDUCTIVE FEATURES, COMPLEMENTARY RECEPTACLE, AND METHODS OF FABRICATION, ASSEMBLY, AND OPERATION THEREFOR

Assignee: Intel Corporation

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Dkt: 884.826US1 (INTEL)

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney, Sherry Schumm at (480) 538-1735, or Applicants' below-named representative at (612) 349-9592 to facilitate the prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By his Representatives,

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Date June 8, 2005

By Ann M. McCrackin

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of June 2005.

Name

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Signature

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